

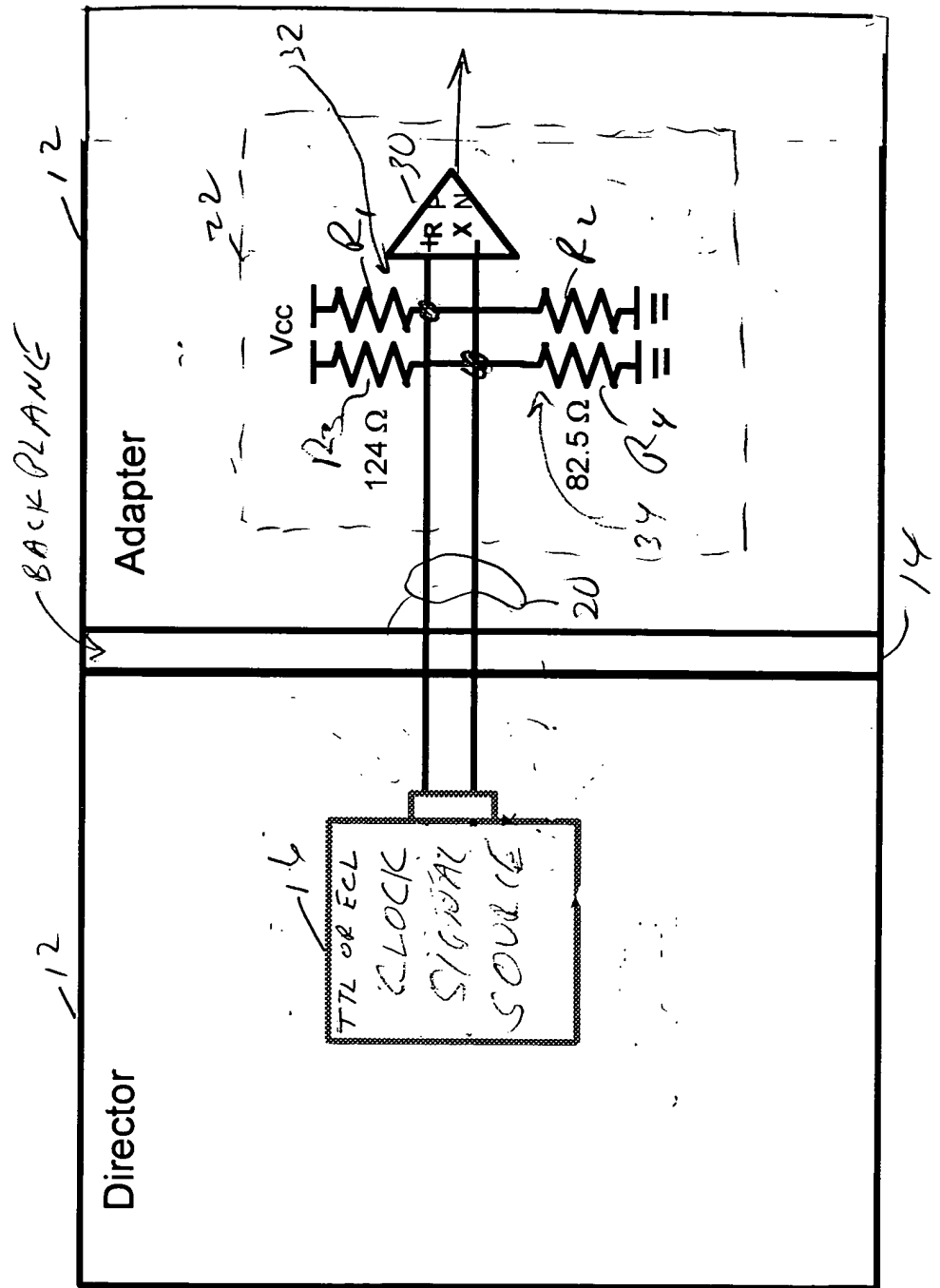
# CLOCK SIGNAL REGENERATION CIRCUITRY

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FIG. 1

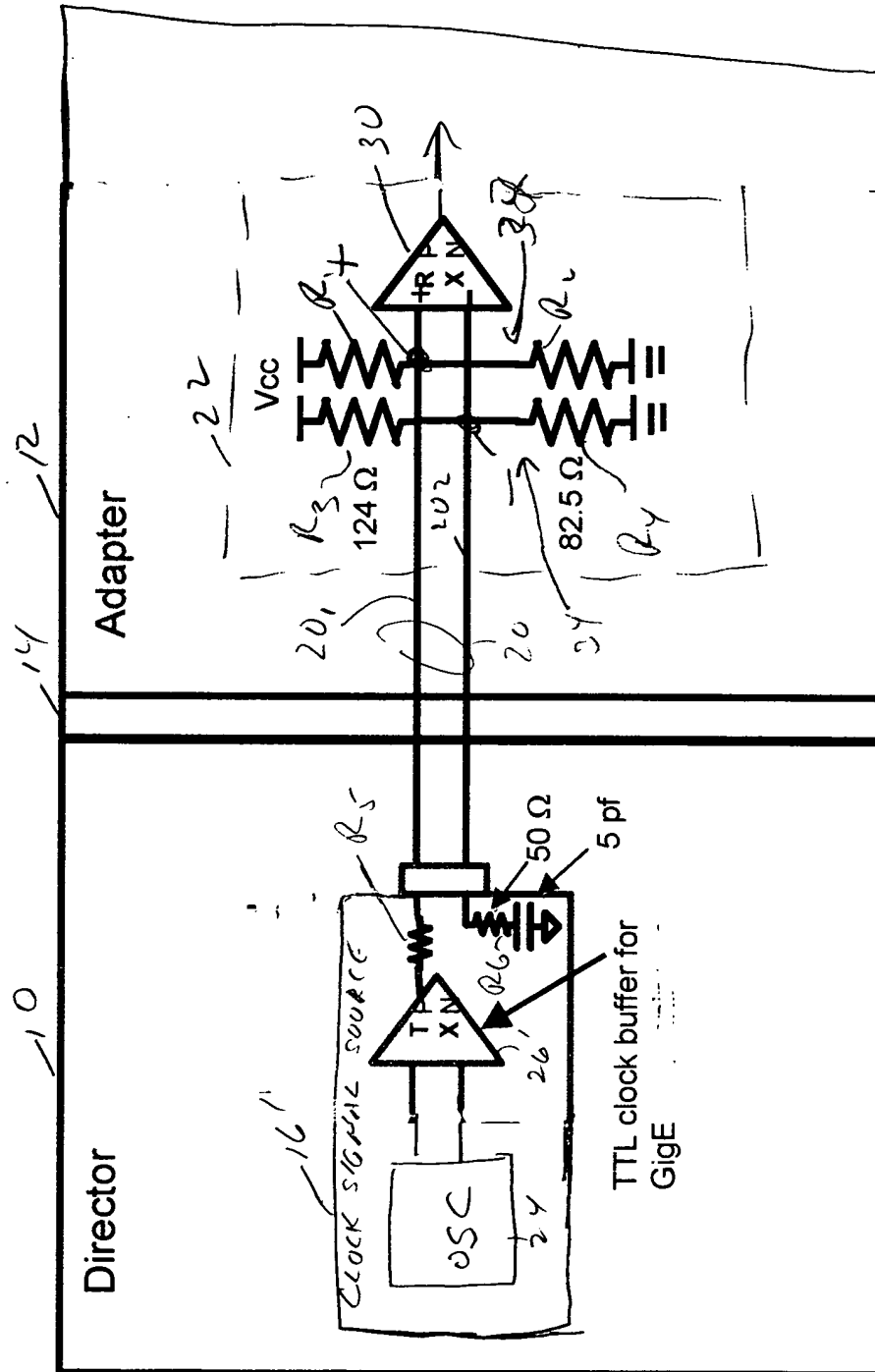


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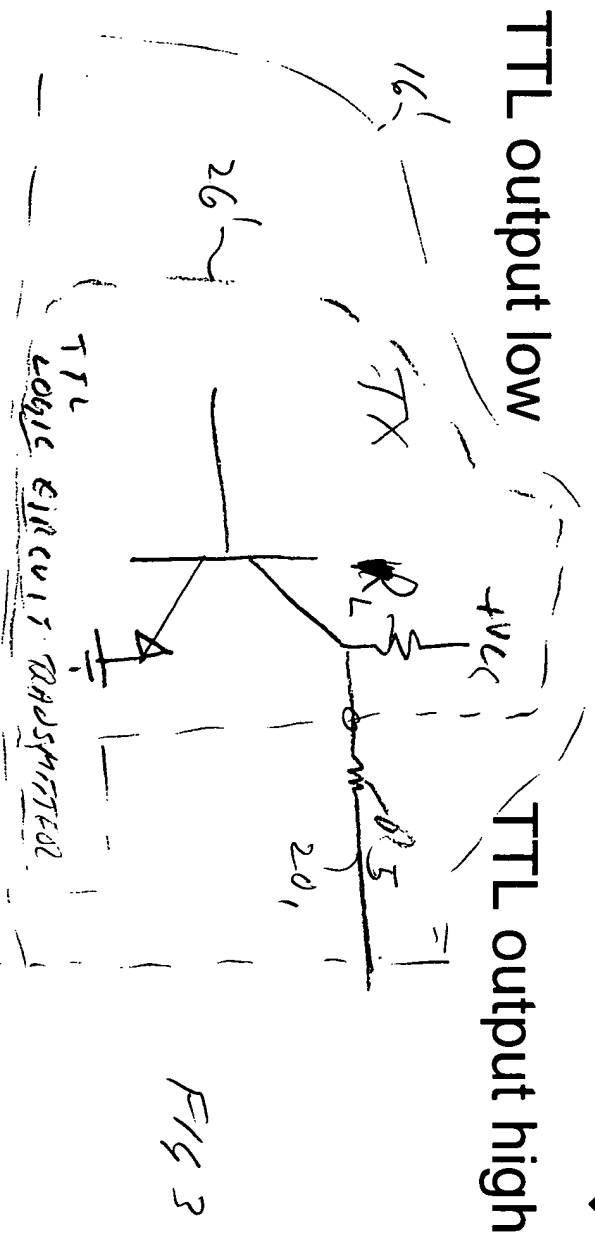
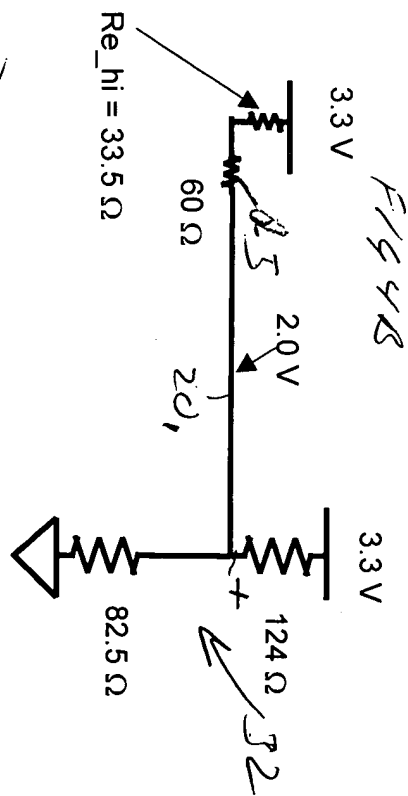
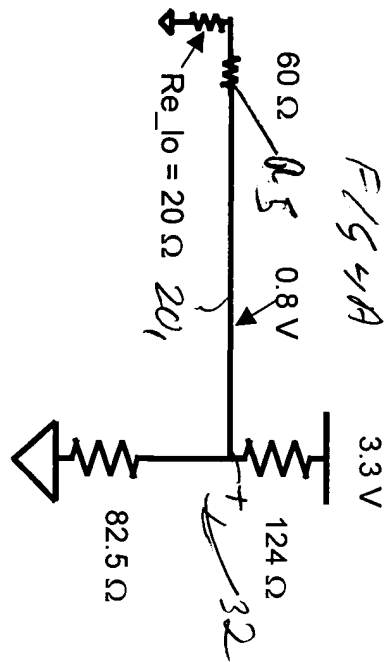
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## Equivalent DC circuit of TTL clock



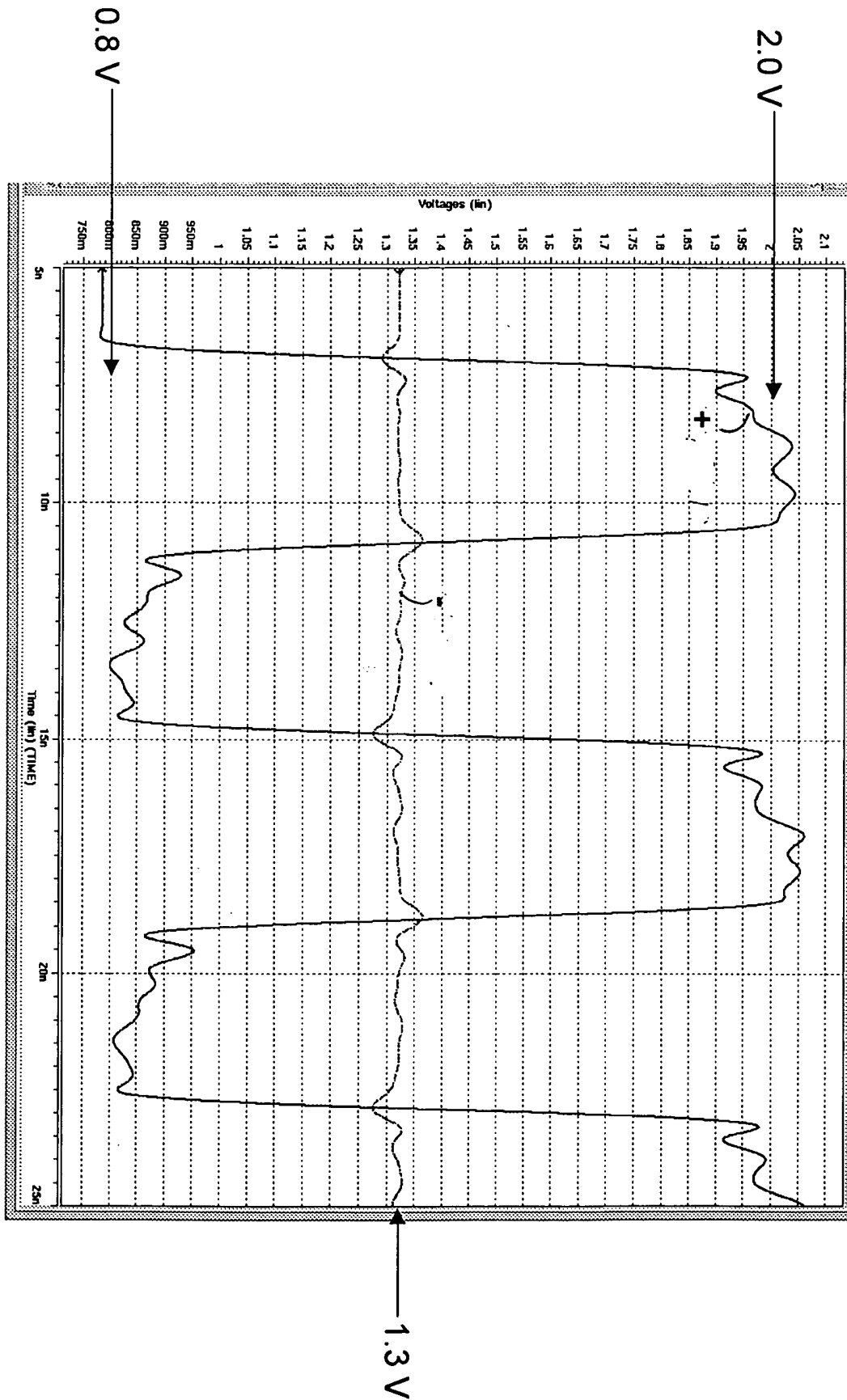
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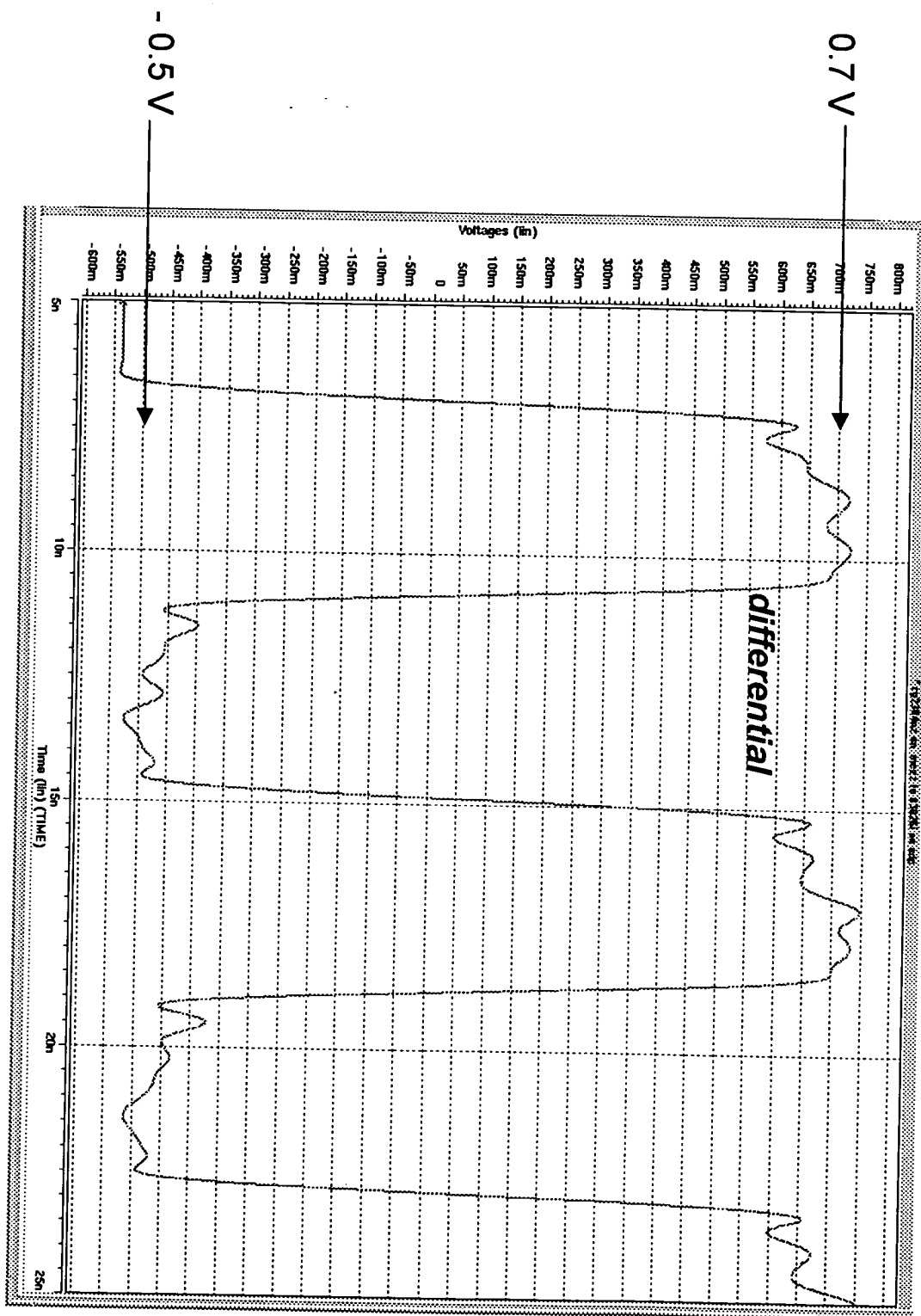
TTL clock inputs (+ and - of RX)

1-15, J



TTL clock inputs ('+' - '-' of RX)

Figs 6.

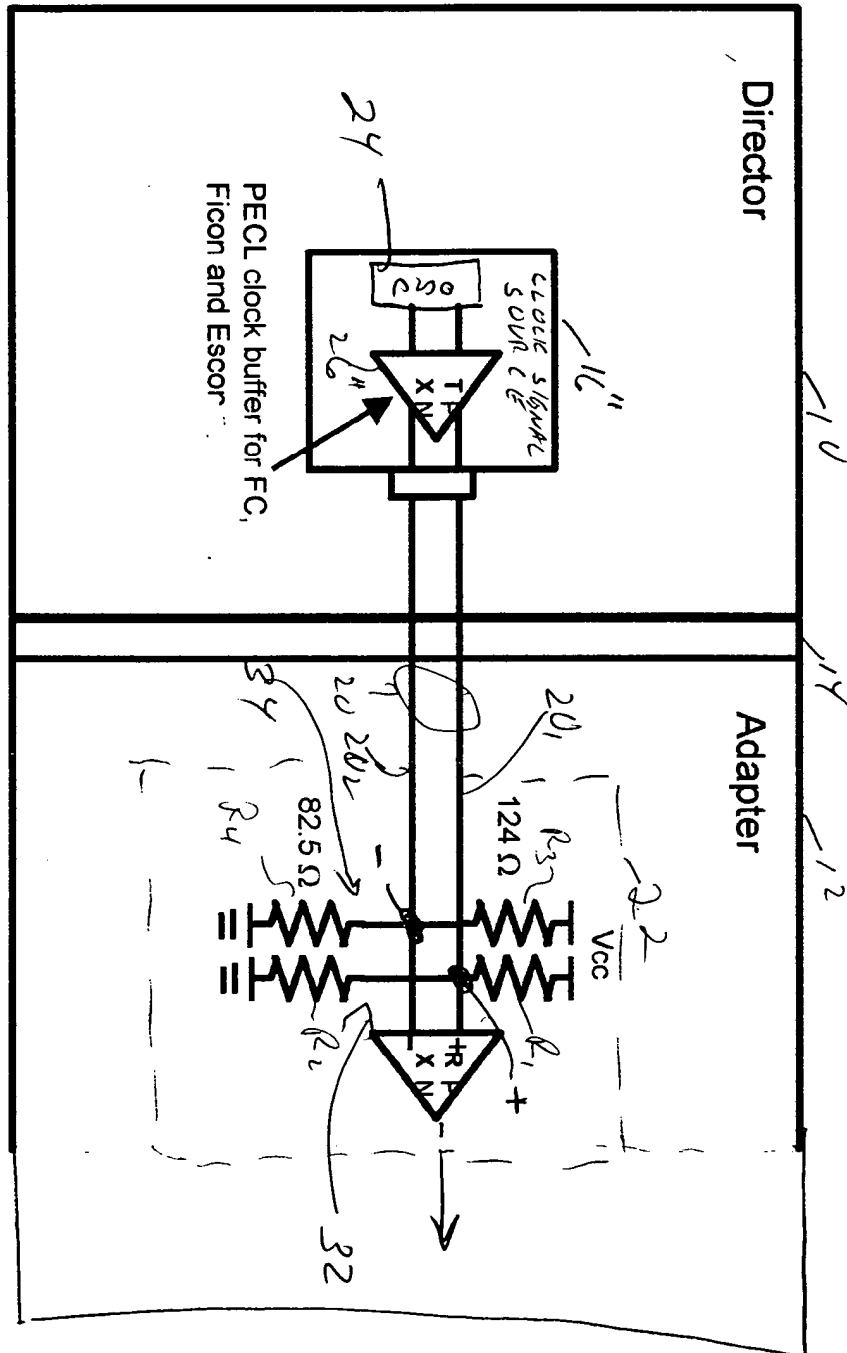


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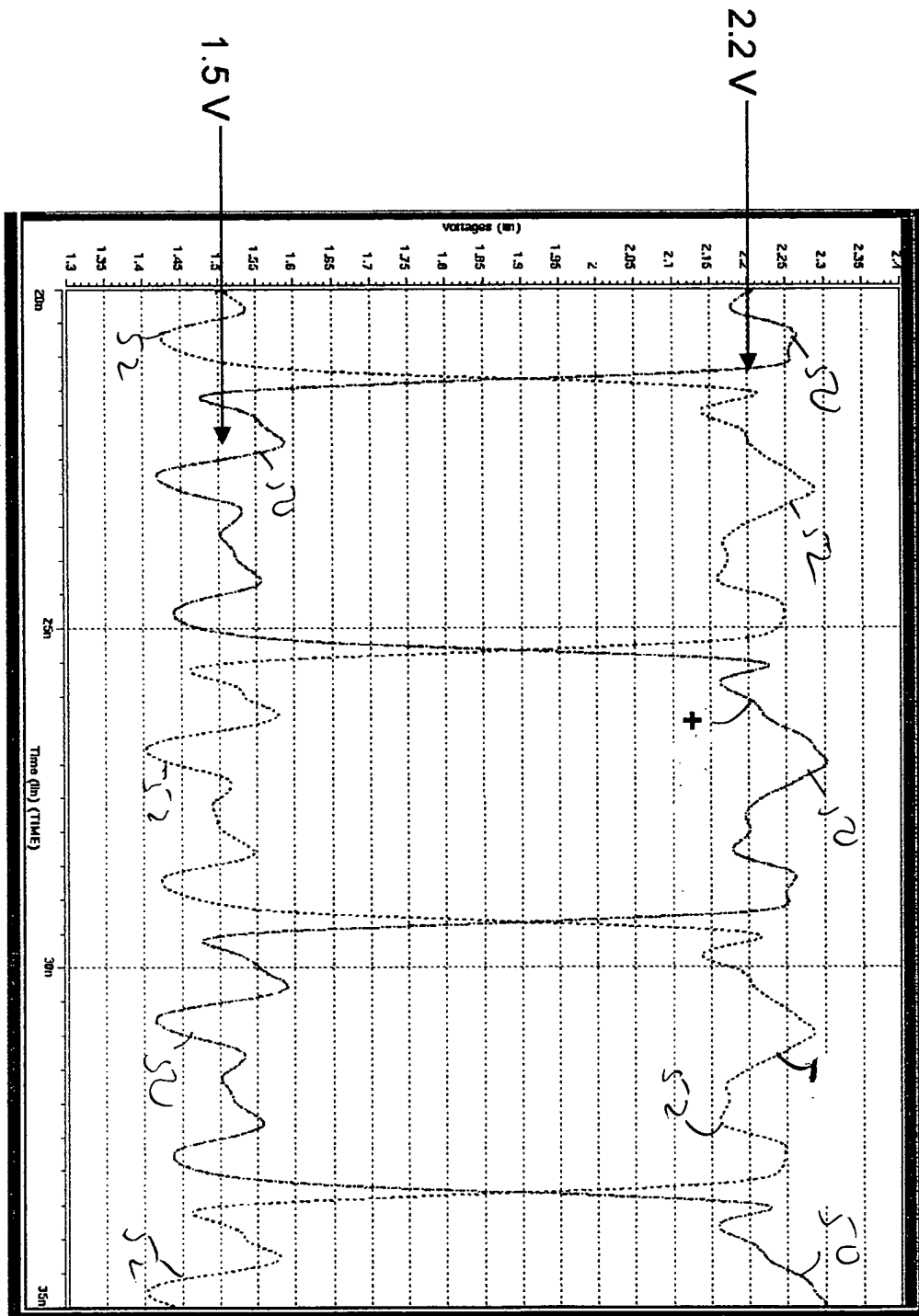
F15.7

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PECL clock input signals (+ and - of RX)



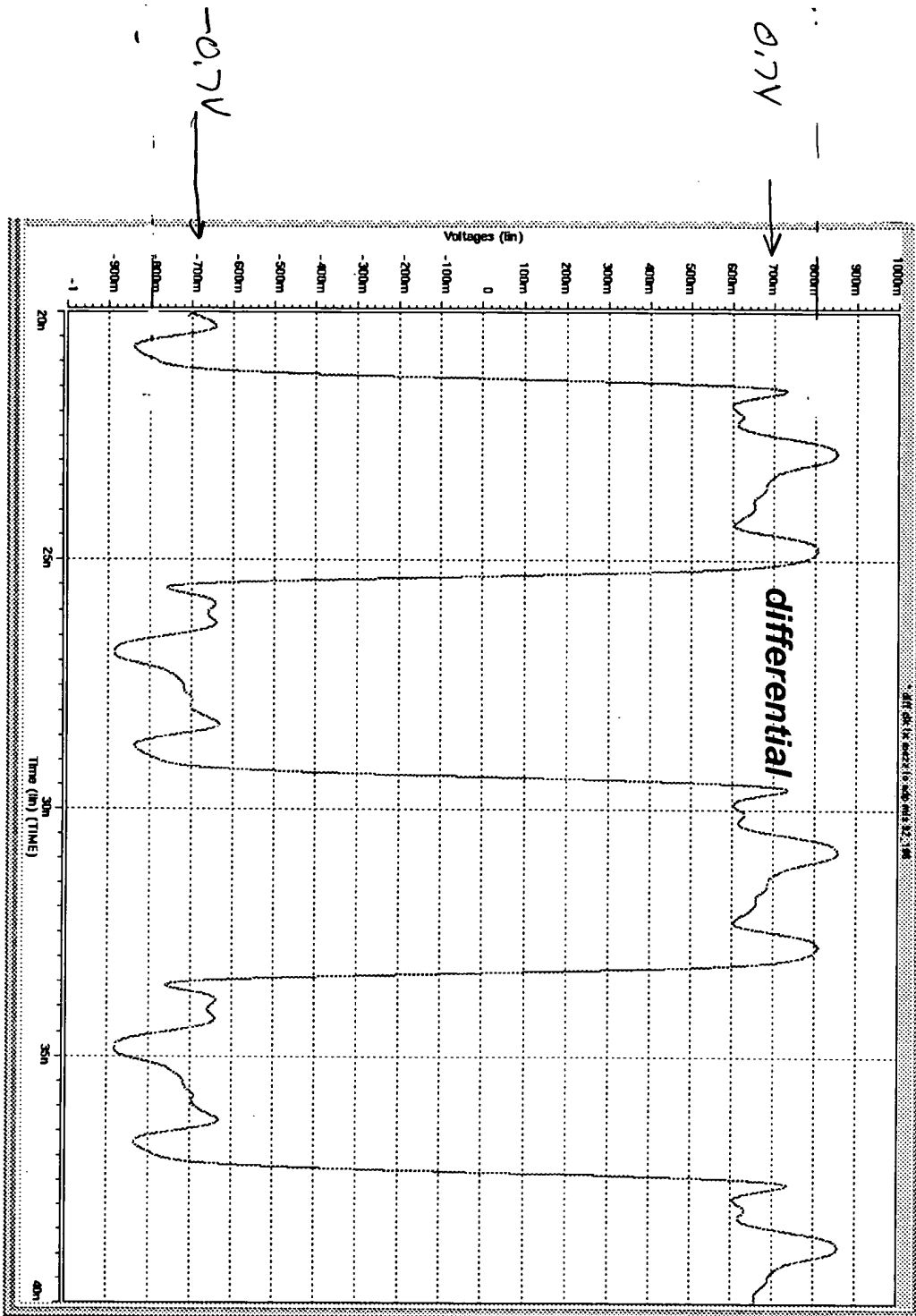
7-19.8

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PECL clock input signals ('+' - '-' side)

F14.9